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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,694	09/23/2003	Anthony Ciancio	SC12836ZP	2205

23125 7590 06/03/2005

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,694	CIANCIO ET AL.	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8,9,11,13,15,16 and 20* is/are rejected.

7)☒ Claim(s) *3,7,10 and 14* is/are objected to.

8)☒ Claim(s) *17-19* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-6, 8, 9, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0011043 Roberts.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

1. Referring to claim 1, a semiconductor device comprising: a semiconductor substrate, (Figure 7 #10), a first electrode, (Figure 7 #14), formed over the semiconductor substrate, (Figure 7 #10); a first conductive smoothing layer, (Figure 7 #16 and Paragraph 0013-0014 and Paragraph 0017 Lines 25-35, where it is being taught the adhesion properties between the dielectric and the electrode, hence creating an interface that is smoother than the metal electrode), formed over the first electrode, (Figure 7 #14), wherein the first conductive smoothing layer, (Figure 7 #16), has a surface roughness less than that of the first electrode,

(Figure 7 #14); a dielectric layer, (Figure 7 #18), formed on the first conductive smoothing layer, (Figure 7 #16); and a second electrode, (Figure 7 #20), formed over the dielectric layer, (Figure 7 #18).

2. Referring to claim 2, a semiconductor device, further comprising: a second conductive smoothing layer, (Figure 7 not shown Paragraph 0020 Lines 11-14), formed between the dielectric layer, (Figure 7 #18) and the second electrode, (Figure 7 #20), wherein the second conductive smoothing layer, (Figure 7 not shown Paragraph 0020 Lines 11-14 and Figure 7 #16 and Paragraph 0013-0014 and Paragraph 0017 Lines 25-35, where it is being taught the adhesion properties between the dielectric and the electrode, hence creating an interface that is smoother than the metal electrode), has a roughness less than that of the second electrode, (Figure 7 #20).

3. Referring to claim 4, semiconductor device, wherein the first electrode, (Figure 7 #14), comprises a first layer comprising a metal and a second layer comprising a refractory nitride, (Paragraph 0016 Lines 13-17), and the second electrode comprises a metal, (Figure 7 #20 Paragraph 0020 Lines 4-10).

4. Referring to claim 5, a semiconductor device, wherein the first electrode, (Figure 7 #14 Paragraph 0016 Lines 13-17), and the second electrode comprise a refractory nitride, (Figure 7 #20 and Paragraph 0020 Lines 4-10).

5. Referring to claim 6, a semiconductor device, wherein the refractory nitride comprises a material selected from the group consisting of titanium nitride and tantalum nitride, (Paragraph 0020 Lines 4-10).

6. Referring to claim 8, a semiconductor device, wherein the dielectric layer comprises a high dielectric constant material, (Figure 7 #18 Paragraph 0018 Lines 9-15).

7. Referring to claim 9, a semiconductor device, wherein the first electrode, the first conductive smoothing layer, the dielectric layer and the second electrode are part of a metal-insulator-metal (MIM) capacitor, (Figure 7 and Paragraph 0014 Line 3).

8. Referring to claim 20, a method for forming semiconductor device comprising: providing a semiconductor substrate, (Figure 7 #10); forming a first electrode, (Figure 7 #14), formed over the semiconductor substrate, (Figure 7 #10); forming a first conductive smoothing layer, (Figure 7 #16), formed over the first electrode, (Figure 7 #14), wherein the first smoothing layer, (Figure 7 #16 and Paragraph 0013-0014 and Paragraph 0017 Lines 25-35, where it is being taught the adhesion properties between the dielectric and the electrode, hence creating an interface that is smoother than the metal electrode), has a surface roughness less than that of the first electrode, (Figure 7 #14); forming a dielectric layer, (Figure 18 #18), formed on the first smoothing layer, (Figure 7 #16); and forming a second electrode, (Figure 7 #20), formed over the dielectric layer, (Figure 7 #18).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,099,701 Liu et al.

9. Referring to claim 11, a semiconductor device comprising: a conductive layer, (Figure 2 #24 & 30), a smoothing layer, (Figure 2 #31), formed in contact with the conductive layer,

(Figure 2 #24 & 30), and the smoothing layer, (Figure 2 #31), comprises titanium rich nitride; wherein the smoothing layer, (Figure 2 #31), has a surface roughness less than that of the conductive layer, (Figure 2 #24 & 30); and a dielectric layer, (Figure 2 #20), formed in contact with the smoothing layer, (Figure 2 #31).

10. Referring to claim 13, a semiconductor device, wherein the conductive layer comprises titanium nitride, (Figure 2 #24 & 30 and Col. 3 Lines 61-62).

11. Referring to claim 15, a semiconductor device, wherein the conductive layer comprises a first layer comprising a metal and a second layer comprising a refractory nitride, (Figure 2 #24 & 30 and Col. 3 Lines 61-62).

12. Referring to 16, a semiconductor device, wherein the dielectric layer is a high, (what is high? There is no reference point to determine what high is. The examiner believes the referenced dielectric is high), dielectric constant material, (Figure 2 #20).

Allowable Subject Matter

13. Claims 3, 7, 10 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 17-19 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
5/24/05